or incorporating highly doped semiconductor material for the source and drain contacts different from the channel material to provide etch selectivity and a T-shaped gate or incorporating a metal for the source and drain contacts and the oxide of the metal for the gate dielectric which is self aligned.--

R E M A R K S

The specification has been amended at page 30, lines 8-11.

The Abstract of the disclosure is objected to because lines 8-11 refers to purported merits of the claimed invention and draws comparison to the prior art. The abstract has been amended to delete the last sentece on lines 8-11. It is respectfully submitted that the abstract as amended complies with the requirements of 37 CFR 1.72.

Claims 30 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kudoh (US patent No. 5,159,416) in view of Coleman, Jr. et al. (US patent No. 4,521,446). Kudoh shows a source and drain of titanium silicide. Kudoh shows a borophosphosilicate glass layer 98 in Figs. 9 and 10 which appears to be a blanket layer covering the source, drain and gate. Kudoh does not show or suggest a first dielectric layer on said source and drain adjacent the channel of the FET in Figs. 9 and 10. Claim 30, lines 5 and 6, recites, "a first dielectric layer on said source and drain adjacent said channel,". The first dielectric layer functions to define the location of the gate dielectric and protect the metal used to form the source and drain metal-semiconductor compound regions when the gate

dielectric is formed. Further, Kudoh does not show or suggest a gate dielectric layer comprising TiO_2. Kudoh merely shows silicon oxide.

Coleman, Jr. et al. is directed to hydrogen annealing to permit deposition of good quality polysilicon atop TiO_2. Coleman, Jr. et al. teaches the addition of TiO_2 over a very thin silicon dioxide gate dielectric to plug pinhole defects in the oxide. Claim 30, lines 7 and 8, recites "a gate dielectric of local reacted metal of said metal used in said metal-semiconductor compound regions on said channel,". Coleman, Jr. et al. does not show or suggest a gate dielectric of local reacted metal of said metal used in said metal-semiconcutor compound regions on said channel.

Claim 33 which contains all limitations of claim 30 further recites "said gate dielectric layer includes TiO_2." Kudoh shows titanium silicide source and drains and a silicon oxide gate dielectric. Coleman, Jr. et al. shows a gate dielectric of silicon oxide improved by forming TiO_2 thereover. The discussions submitted for the patentability of claim 30 are herein incorporated for the patentability of claim 33. It is respectfully submitted that claims 30 and 33 are patentable over Kudoh in view of Coleman, Jr. et al.

Further favorable action and allowance of the claims is earnestly requested.

Respectfully submitted,
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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification:

Paragraph beginning at line 3 of page 30 has been amended as follows:

A field effect transistor and method for making is described incorporating self aligned source anjd drain contacts with Schottky metal-to-semiconductor junction and a T-shaped gate or incorporating highly doped semiconductor material for the source and drain contacts different from the channel material to provide etch selectivity and a T-shaped gate or incorporating a metal for the source and drain contacts and the oxide of the metal for the gate dielectric which is self aligned. [The invention overcomes the problem of self-aligned high resistance source/drain contacts and a high resistance gate electrode for submicron FET devices which increase as devices are scaled to smaller dimensions.]